INVERTER CONTROLLER

Field of the Invention

The present invention relates to an inverter controller, and more particularly, to an inverter controller that utilizes pin multiplexing and/or pin multitasking techniques to reduce the overall pin count and reduce the number of components, without reducing the functionality and/or performance of the controller. Particular utility for the present invention is for a two-switch DC/AC inverter topology for driving a CCFL, however, other inverter topologies and/or DC/DC converter topologies, and/or other loads are equally contemplated herein.

SUMMARY OF THE INVENTION

The present invention provides an integrated circuit that includes an inverter controller being adapted to generate a plurality of signals to drive an inverter circuit. The controller also includes one or more input pins configured to receive two or more input signals. Each signal supports an associated function of the controller.

In one exemplary embodiment, the input pin is configured to receive a first signal representing a dim voltage, where the first signal has a first voltage range. The pin is also configured to receive a second signal representing a voltage feedback signal, where the second signal has a second voltage range.

In another exemplary embodiment, the input pin is configured to receive a first signal representing a current feedback signal, where the first signal is present in a first time period. The pin is also configured to receive a second signal representing a soft-start signal, where the second signal is present in a second time period.

The present invention also provides an inverter controller IC that includes a multiplexer circuit to direct one input signal to a first circuit to support a first function of the controller, and to direct another of the input signals to a second circuit to support a second said function of the controller.

The present invention further provides an inverter controller IC that includes an input pin configured to receive two or more input signals, each signal supports an associated function of the controller. One of the input signals is present in a first time period and another of the input signals is present in a second time period.

Thus, according to the present invention pin count may be significantly reduced. Also, by choosing which pins may be multifunctional and/or multiplexed, the present invention decreases tooling and PCB layout requirements.

Additional benefits and advantages of the present invention will become apparent to those skilled in the art to which this invention relates from the subsequent description of the preferred embodiments and the appended claims, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of one exemplary inverter controller integrated circuit according to the present invention;

Figure 2 is a block diagram of another exemplary inverter controller integrated circuit according to the present invention;

Figure 3 depicts an exemplary application circuit topology for the inverter controller IC of Figures 1 or 2;

Figure 4 depicts another exemplary application circuit topology for the inverter controller IC of Figures 1 or 2;

Figure 5 depicts representative signal graphs for certain signals generated by the controller of Figure 1; and

Figure 6 depicts representative signal graphs for certain signals generated by the controller of Figure 2.

Detailed Description of Exemplary Embodiments

Figure 1 depicts a block diagram of an exemplary inverter controller integrated circuit 10 according to the present invention. In this exemplary embodiment, the controller 10 is an 8 pin design (labeled 1-8), where pin 2 is adapted to receive two signals and multiplexed to support two functions, and pin 4 is adapted to receive two signals to support two functions, depending on the state certain components of the controller. In this example, pin 2 supports both load voltage sensing and dim signal sensing. Pin 4 supports both current comparing during normal operating conditions and soft start (SST) operation during initial turn on and/or lamp out conditions.

The controller 10 includes an overvoltage protection circuit 100, a dimming circuit 200, a current feedback control circuit 300 and an output circuit 400. The controller 10 also includes a MUX 18 to control switching of the function of PIN 2 between load voltage sensing and dimming signal input control, based on the state of the load. The controller also includes an oscillator circuit 12 that generates a sawtooth signal 14 by charging/discharging a fixed capacitor CT 16, and a reference signal/ bias signal generator 20 that generates one or more of the reference and/or bias signals utilized by the controller 10. The controller operates to generate two switch driving signals NDR1

and NDR2. The drive control signals may be used to drive the two switches of a derived Royer circuit, a push pull circuit, a half bridge circuit or other two-switch inverter circuit known in the art.

Stated another way, the present invention provides an inverter controller that includes a one or more multiplexed and/or multifunctional pins, where the controller is adapted to generate one or more control signals based on the signal state of the multiplexed and/or multifunctional pins. The following description of the overvoltage protection circuit 100, the dimming circuit 200, the current control circuit 300 and the output circuit 400 will be readily understood by those skilled in the inverter arts. Each of the components of the controller 10 is described in greater detail below.

Output circuit 400 includes a comparator 42 that compares a signal 52 from the output of the error amplifier 30 with a sawtooth signal generated by the oscillator circuit 12. The error signal 52 is generated by the current control circuit 300 and/or the CMP capacitor 40 (at PIN 4), as also may be modified by the dimming circuit 200. The error signal has a value to be within the range of the minimum and maximum value of the sawtooth signal 14 for normal operation. For example, for CCFL loads, the sawtooth signal may have a range between 0V and 3.0V. As is understood in the art, the intersection between the sawtooth signal 14 and the error signal 52 is used by the switch driver logic 44 to set the pulse width of each of the switch driver signals NDR1 and NDR2. Generally, the higher the error signal value, the wider the pulse width and thus, more power is delivered to the load (although the circuitry could be modified where the reverse is true).

As set forth above, the value of the error signal 52 is determined by current feedback information generated by the current control circuit 300, and modified by the dimming circuit 200. As a general matter, The CMP capacitor 40 is charged during the initial power on of the controller 10. Error amplifier 30 operates as a current source (e.g., transconductance amplifier) to adjust the charge on the CMP capacitor 40. Amplifier 30 compares the load current Isens to a user-definable reference signal 32 indicative of maximum load current at maximum power or maximum brightness 32. If the value of the load current is less than signal 32, amplifier 30 will source current to charge the capacitor 40 in an attempt to increase the DC value of the error signal 52, thereby increasing the pulse width of the output driver signals NDR1 and NDR2. If the value of the load current is greater than the reference signal 32, amplifier 30 will sink charge from the CMP capacitor 40 to decrease the DC value of the error signal 52, thereby decreasing the pulse width of the output driver signals NDR1 and NDR2. In other words, amplifier 30 represents a closed loop feedback current control that sources or sinks current to attempt to maintain the load current Isens approximately equal to the reference signal 32.

Dimming circuitry 200 is enabled by the MUX circuit 18 (a process that is described in greater detail below), the relative dim value is set by VDIM (PIN 2). In the exemplary embodiment, VDIM is a DC signal having a value between V1 and V2. VDIM may be generated by a software programmable dimming value or a switch (e.g., rotary switch) operated by a user. In this example, the greater the value of Vdim, the more power is delivered to the load although the circuitry could be modified where the reverse is true. Dimming circuitry 200 is a burst mode dimming circuit that generates a burst mode signal (low frequency PWM signal 50) that its duty cycle is proportional to

Vdim. The frequency of the burst mode signal 50 is selected to be far less than the frequency of the driving signals NDR1 and NDR2. For example, for CCFL applications the typical operating range of the driving signals is 35-80 kHz, and the burst mode signal may have a frequency of approximately 200 Hz.

In the exemplary embodiment, dimming circuit 200 comprises a digital dimming circuit that receives Vdim and converts Vdim to a digital signal. The digital signal is weighted to a predetermined bit depth (e.g., 8 bit) to render a predetermined number of dimming values (e.g., 256 dim levels). The digital dimming circuit 36 generates a burst mode signal 50 that has a duty cycle proprtial to the value of Vdim. In this example, the duty cycle of the burst mode signal 50 ranges from 0% (Vdim=V1) to 100% (Vdim=V2).

If the dimming circuit 200 is enabled by the MUX 18, the PWM enable block 38 operates to sink charge from the CMP capacitor 40. The enable block 38 may comprise a simple switch tied to ground whose conduction state is controlled by the burst mode signal 50. As stated above, error amplifier 30 generates an output to maintain a DC signal 52 having a maximum value represented by signal 32. The burst mode signal 50 operates as follows. When the burst mode signal is asserted (high or low), the enable circuit 38 sinks the charge from the capacitor 40. The resulting DC signal 52 is a minimum value (e.g., 0 Volts). As a result, the signal generated by comparator 42 represents the intersection between the lowest value of the CT signal 14 and the DC signal 52, and accordingly the switch driver logic 44 turns the driving signals NDR1 and NDR2 off while the burst mode signal is asserted. When the burst mode signal is deasserted, the enable block essentially becomes an open circuit and the error amplifier 30 recharges capacitor 40 to the original value. The resulting error signal resumes to

the value corresponding to the maximum brightness output as described above, and accordingly the switch logic driver generates driving signals NDR1 and NDR2 having a duty cycle corresponding to the maximum brightness output . Thus, burst mode operation, in this exemplary embodiment swings the output from fully on to fully off at a frequency determined by the burst mode signal 50.

PIN 2 is adapted to receive two signals representing both load voltage sensing (Vsens) and DIM signal input. The DIM signal (Vdim) is used to support power control of the load. Load voltage control is used, for example, to detect an overvoltage condition at the load. In this example, a multiplexer MUX 18 is ustilized to direct the input on PIN 2 (either Vsens or Vdim) into the overvoltage protection circuit 100 or the dimming circuit 200, based on a predetermined condition. In this example, the predetermined condition is a lamp on signal 34 which indicates that a lamp load is present and working properly, where signal 34 is an input to the MUX 18. In this exemplary embodiment, the DIM signal is fixed to a predetermined range, i.e., V1<Vdim<V2. Vsens is configured to be outside this range , i.e., Vsens>V2, or Vsens<V1.

When the controller is initially powered on to drive a load, the controller will receive both load voltage and load current feedback to determine if the load is operating properly. Current feedback is represented by Isens at PIN 3, and voltage feedback is represented by Vsens at PIN 2. Assuming a lamp load (e.g., CCFL), those skilled in the art will recognize that a broken or missing lamp can create a dangerously high voltage situation at the secondary side of a transformer (not shown in Figure 1). Thus, the present invention initially determines the status of the lamp load by checking if a minimum current is being delivered to the load.

To that end, comparator 28 compares the load current Isens with a lamp threshold signal 46. The lamp threshold signal 46 is a signal indicative of the minimum current that should be present at the load if the load is working properly. If Isens is greater than or equal to signal 46, comparator 28 generates a lamp on signal 34 indicative that the load is properly working. The lamp on signal 34 is a control signal generated by the comparator 28 that controls the state of the MUX 18. In this case, the lamp on signal sets the output state of the MUX to couple the dimming circuitry 200 to PIN 2. A latch circuit 74 is provided to latch the output of the lamp on signal once Isens exceeds the threshold signal 46. The lamp on signal will remain in this state during normal operation, so that burst mode dimming (described below) does not change the state of the lamp on signal. The Vdim input on PIN2 is then used to set the desired dim brightness value (as will be described below).

If, however, during the time when the controller is initially powered to drive the load (and before the latch circuit 74 is set), the current sense value Isens stays below the lamp threshold signal 46, the output of the amplifier 28 changes the state of the lamp on signal 34. This, in turn, changes the state of the MUX to couple the overvoltage protection circuit 100 to PIN 2. As is understood in the CCFL arts, Vsens is derived from the secondary side of the transformer used to drive the lamp load. Under normal operating conditions, Vsens will not affect the range of Vdim, i.e., V1<Vdim<V2. If, however, and open or broken lamp condition exists, Vsens will rise to a value greater than V2. When PIN 2 is coupled to the overvoltage protection circuit 100, Vsens is compared to a predetermined overvoltage threshold signal Vovp (where Vovp>V2) in

comparator 22. When Vsens exceeds Vovp 48, the output of comparator causes timing circuit 24 to initiates a predefined timeout period.

Since this is a broken or missing lamp condition, Isens will have a value less than the lamp threshold signal 46. Also, error amplifier 30 will generate an output signal in an attempt to source the CMP capacitor to increase the power delivered to the load. Accordingly, during the timout period, the protection circuit operates in a manner similar to the PWM enable circuit 38. During this period, to prevent the error amplifier from generating a error singal to cause the switches to drive at higher power, the OVP signal 60 stops the error amplifier 30 to charge/discharge of CMP capacitor 40 At the end of the timout, the protection circuit 26 disables the switch driver logic 44 and thus the output overvoltage is controlled.

Thus, to summarize, the present invention provides an inverter controller IC for generating power to a load that includes: 1) an overvoltage protection circuit 100 configured to receive a voltage feedback signal from the load and configured to generate a protection signal to discontinue power to the load, 2) a dimming circuit 200 configured to receive a dimming signal and configured to generate a dimming signal to control the power delivered to the load, 3) a current control circuit 300 configured to receive a current feedback signal from the load and configured to generate an error signal; and an output circuit 400 configured to receive said error signal and said dimming signal and configured to generate drive signals for driving said load. One of the IC pins (e.g., PIN 2) is configured to receive the voltage feedback signal and the dimming signal. A multiplexer 18 coupled to the pin and configured to direct the voltage feedback signal to

the overvoltage protection circuit or the dimming signal to the dimming circuit, based on the value of the current feedback signal.

PIN 4 and the CMP capacitor also operates to control soft start (SST) functionality. Soft start, as is known in the art, essentially operates in the beginning of power on, to cause the output circuitry to generate a minimal pulse width and gradually increase the pulse width. At initial power on the voltage on the CMP capacitor is zero. Isens is also zero, and therefore the error amplifier attempts to source the CMP capacitor to a charge that satisfies signal 32. The time this process takes is dependent on the desired charge on CMP and the capacitance of CMP, and therefore this time period is utilized as soft start. This ensures that the amount of power to the load is increased gradually. It continues until the load current value reaches the threshold value 32. Then the error amplifier 30 takes over the control of PIN 4 which is the charge on the capacitor, as described herein. For CCFL loads, it is known that a gradual increase in lamp current helps to ensure the life of the lamp.

Thus, PIN 4 is adapted to generate the DC signal CMP 52 based on the values of the error signal generated by the current control circuit 300 and/or the dimming signal generated by the dimming circuit 200. PIN 4 is multifunctional since it is also adapted to generate a soft start signal 52 based on the value of the error signal generated by the current control circuit 300.

Figure 5 depicts representative signal graphs for certain signals generated by the controller 10 of the present invention. Figure 5A shows the drive signals NDR1 and NDR2. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP 52 and the sawtooth signal CT, as depicted in Figure 5D. Figure 5B

depicts the burst mode signal (LPWM) 50, and Figure 5C depicts the load current I_L. When the burst mode signal is deasserted (high) 50A, the drive signals and lamp current are present. When the burst mode signal is asserted (low) 50B, the drive signals stop and the lamp current is approximately zero. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (approximately zero) as described above.

Figure 2 depicts another exemplary inverter controller 10' according to the present invention. The inverter controller 10' of this exemplary embodiment operates in a similar manner as described above with reference to Figure 1, but includes additional circuitry which may be desirable for a given operating environment. For example, at the output of error amplifier 30 is an on/off circuit triggered by the OVP signal. If the overvoltage protection circuit is activated, the OVP signal shuts the output of the error amplifier 30 off, regardless of the value of Isens. Thus, when the OVP signal is asserted, the capacitor 40 is discharged by the protection circuit 26 so that the output signals NDR1 and NDR2 operate in a minimum state to deliver minimum power. Of course, the protection circuitry may also be adapted to charge the capacitor 40 to some minimum level so that the output signals deliver a predetermined minimum pulse width to the load during the time out period.

The controller 10' also includes a min/max circuit 56 which, during times when the burst mode signal is enabled , generates a minimum DC value (instead of a zero DC value 52, as described above during these periods). Thus, the intersection between the sawtooth signal and the minimum DC signal generated by the min/max circuit 56 generates an output to cause the output signals to have some predetermined minimum pulse width. This prevents, for example, wide voltage swings and/or maintain continuous

function of the drive signals between burst mode signal asserted and burst mode signal deasserted.

An enable comparator 58 is provided to generate an enable control signal to the switch logic 44. The comparator generates an enable signal (thereby enabling the switch logic) if the value on the capacitor 40 is greater than the enable threshold value or else the switch logic is disabled.

The PWM enable circuit 38' may include a floor value (i.e., bias), below which the enable circuit will not sink charge from the CMP capacitor 40. Like the min/max circuit, this prevents the burst mode enabled signal from completely sinking the charge on the capacitor, so that the output signals are set at a predetermined minimum other than zero. The value of the bias may be selected in accordance with the operating range of the controller, a desired minimum power delivered to the load during burst mode assertion, and/or other factors that will be apparent to those skilled in the art.

Figure 6 depicts representative signal graphs for certain signals generated by the controller 10' of the present invention. Figure 6A shows the drive signals NDR1 and NDR2. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP 52 and the sawtooth signal CT, as depicted in Figure 6D. Figure 6B depicts the burst mode signal (LPWM) 50', and Figure 6C depicts the load current I_L. When the burst mode signal is deasserted (high) 50A', the drive signals and lamp current are present. When the burst mode signal is asserted (low) 50B', the drive signals are reduced to a predetermined minimum pulse width and the lamp current is significantly reduced. The asserted value of the burst mode signal 50B' is biased in a manner

described above. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (greater than zero), as described above.

Thus, the exemplary inverter controller ICs 10 and 10' of Figures 1 and 2 include a pin (e.g., PIN2) that is multiplexed to receive a first input signal (e.g., Vdim or Vsens) with a first predefined range, and a second signal with a second predefined range. The inverter controller ICs 10 and 10' are also adapted to include a pin (e.g., PIN 4) that is multifunctional to operate is a first time period (e.g., normal operating conditions) and a second time period (e.g., initial power using soft start loading).

Figure 3 depicts an exemplary application topology for the inverter controller IC 10 or 10'. The controller IC 10 or 10' depicted in Figure 3 is used to drive a derived Royer circuit comprised of transistors Q1 and Q2, to power a CCFL load 66. Q1 and Q2 drive the primary side of the transformer 60, through a resonant tank circuit formed by the capacitor 68 and the primary side inductance of the transformer 60. The operation of this type of circuit is well known by those skilled in the art. Vsen is derived from a voltage divider between capacitors C1 and C2 (node 62) so that the value of Vsen is nominal compared to the voltage at the secondary side of the transformer. Vsen is typically in the range of 1 to 5 Volts. Isen is derived from the CCFL load through the divider circuit of R1 and R2 (node 64). Isen will typically range between 0 Volts (no lamp) to 1.25 Volts (full lamp brightness). Of course, these values are only exemplary, and may be modified to meet design criteria without departing from the present invention. Figure 4 represents another exemplary application topology for the inverter controller 10 or 10'. The controller in this embodiment is used to drive two (or more)

CCFL loads 66 and 70. In this case, current feedback Isens is derived from both lamps 66 and 70 from the voltage dividers R1, R2 and R3, R4.

Those skilled in the art will recognize numerous modifications that may be made to the present invention. For example, the controller ICs 10 and 10' of Figures 1 and 2 multiplex the values of Vsen and DIM on PIN 2, and combine the functionality of the charge capacitor CMP 40 and soft start functionality. However, these are only examples of pin multiplexing/multitasking that may be accomplished by the present invention. Other pins associated with the exemplary IC may be multiplexed and/or multitasked. Additionally, other IC designs that require more or fewer pins than the 8 pin IC depicted in Figures 1 and 2 may likewise include pin multitasking and/or multiplexing as provided herein.

Still other modifications may be made. In the exemplary controller ICs of Figures 1 and 2, PIN 2 is multiplexed to support both load voltage sensing and dim signal input. The range of dim signals (V1<Vdim<V2), as disclosed above, and the overvoltage protection threshold Vovp are selected such that Vovp>V2. However, this relationship is not required for the present invention to operate properly. Indeed Vovp may be selected within or below the range of Vsens, since the Vsens value is used by the overvoltage protection circuit 100, independent of the dim value. Alternatively, the multiplexed and/or multifunctional pins disclosed herein may be adapted to support three or more signals, using multiplexing and or multifunctional techniques provided herein.

Still other modifications may be made. For example, the exemplary application topologies of Figures 3 and 4 depict the controller ICs 10 or 10' driving a derived Royer circuit formed by Q1 and Q. However, the controller 10 or 10' may be likewise applied

to a push-pull inverter, a half bridge inverter and/or or other type of two switch inverter topology known in the art. Yet further, the controller IC 10 or 10' may be modified to include a second pair of drive signals (e.g., PDR1 and PDR2) to enable the controller IC 10 or 10' to drive a four switch inverter topology (e.g., full bridge inverter).

The present invention is not limited to a CCFL load. Indeed the controller 10 or 10' of the present invention may be used to drive other lamp loads, such as metal halide or sodium vapor. Still other loads may be used. For example, the controller 10 or 10' of the present invention may be adapted to operate in a frequency range to support driving an x-ray tube or other higher frequency load. The present invention is not limited to the load type, and should be construed as load independent. Additionally, for multiple lamp topologies such as depicted in Figure 4, numerous other topologies may be used, for example as described in U.S. Patent No. 6,104;146, and U.S. Patent Application Serial Nos. 09/873,669, 09/850,692, and 10/035,973, all of which are encorporated by reference in their entirety.

A detailed discussion of the operation of certain components of Figures 1 and 2 has been omitted. For example, the operation of the oscillator circuit 12 and the operation of the switch logic 44 have been omitted since it is assumed that one skilled in the art will readily recognize both the operation and implementation of these features. Also, the timing of the drive signals NDR1 and NDR2 is not described at length herein, since the operation of these signals will be apparent to those skilled in the art. The preceding detailed description of the block diagrams of Figures 1 and 2 is largely directed to the functionality of the components. The components of Figures 1 and 2 may be off-the-shelf or custom components to achieve the functionality stated herein, and those

skilled in the art will readily recognize that many circuit implementations may be used to accomplish the functionality stated herein, and all such alternatives are deemed within the scope of the present invention.

Still further, inverter controller circuits that include voltage and current feedback, and dimming control (as described herein) are well known to those skilled in the art. However, the prior art integrated circuit inverter controllers have failed to address the long-felt need to reduce the IC package pin count while maintaining the functionality of the inverter IC. The present invention described herein provides examples of addressing this issue by providing, for example, multiplexed and/or multifunctional IC pins. Numerous modifications to this inventive theme will be apparent to those skilled in the art, and all such modifications are deemed within the scope of the present invention, as set forth in the claims.